Customer No.: 31561
Application No.: 10/064,644
Docket No.: 9223-US-PA

AMENDMENTS

Please amend the application as indicated hereafter.

In the Title:

Please change the title of the invention to "FLIP-CHIP DIE FOR JOINING WITH A FLIP-CHIP SUBSTRATE."

In the Claims:

1-15 (canceled)

16. (currently amended) A flip chip die for joining with a flip-chip package substrate, wherein the flip chip die having an active surface thereon, comprising:

a group of core die pads on the active surface; and

a plurality of die pad rows on the active surface sequentially laid outside the group of core die pads such that one end of each of the die pad rows is adjacent to the group of core die pads and each die pad row includes a plurality of die pads therein, wherein the die pad rows include ~~are selected from~~ signal die pad rows, power die pad rows and ground die pad rows.

17. (previously amended) The flip chip die of claim 16, wherein the group of core die pads includes a plurality of core power die pads and core ground die pads.

18. (previously amended) The flip chip die of claim 16, wherein at least one signal die pad row is positioned between the power die pad row and the ground die pad row.

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19. (currently amended) A flip chip die for joining with a flip-chip package substrate, wherein the die having an active surface thereon, comprising:

a group of core die pads on the active surface;

a plurality of inner die pad rows on the active surface sequentially laid outside the group of core die pads, wherein a first end of each of the inner die pad rows is adjacent to the group of core die pads and each inner die pad row has a plurality of inner die pads therein, wherein the inner die pad rows include ~~are selected from~~ signal die pad rows, power die pad rows and ground die pad rows; and

a plurality of outer die pad rows on the active surface laid outside a second end of each of the inner die pad rows and vertical to the inner die pad rows, wherein each outer die pad row has a plurality of outer die pads therein.

20. (previously amended) The flip chip die of claim 19, wherein the group of core die pads includes a plurality of core power die pads and core ground die pads.

21. (previously amended) The flip chip die of claim 19, wherein at least one signal die pad row is positioned between the power die pad row and the ground die pad row in the inner die pads rows.

22. (previously amended) The flip chip die of claim 19, wherein the outer die pads are signal die pads.

23. (previously added) The flip chip die of claim 16, wherein each die pad has a bump thereon.

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24. (previously added) The flip chip die of claim 16, wherein the flip-chip package substrate is a multi-layer substrate and has a plurality bump pads at a surface of the package substrate corresponding to the die pads of the flip chip die respectively.

25. (previously added) The flip chip die of claim 19, wherein each die pad has a bump thereon.

26. (previously added) The flip chip die of claim 19, wherein the flip-chip package substrate is a multi-layer substrate and has a plurality bump pads at a surface of the package substrate corresponding to the die pads of the flip chip die respectively.

27. (previously added) The flip chip die of claim 19, wherein the outer die pad rows includes a first outer die pad row, a second outer die pad row and a third die bump pad row sequentially from inside to outside, wherein the shortest distance between the neighboring outer die pads of the second outer die pad row is wide enough to permit the passage of at least one conductive trace at a surface of the package substrate, the shortest distance between the outer die pad of the second outer die pad row and the outer die pad of the third outer die pad row is wide enough to permit the passage of at least one conductive trace at a surface of the package substrate, and the shortest distance between the neighboring outer die pads of the third outer die pad row is wide enough to permit the passage of at least two conductive traces at the surface of a package substrate.

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